AMENDMENTS TO THE CLAIMS

The following listing of claims will replace all prior versions and listings of claims in the application.

LISTING OF CLAIMS

1-46 (Cancelled).

47. (Currently Amended) An amplifier apparatus, comprising:

a plurality of amplifier cells,

wherein each of the plurality of amplifier cells includes (i) ~~an~~ at least one first input in communication with a common ~~source of a~~ control ~~signal~~ voltage, (ii) a second input in communication with a control signal, and ~~(ii)~~ (iii) an output,

wherein the plurality of amplifier cells are arranged in parallel,

wherein the first input of each of the plurality of amplifier cells is in communication with the first inputs of other ones of the plurality of amplifier cells,

wherein the output of each of the plurality of amplifier cells is in communication with the outputs of other ones of the plurality of amplifier cells,

wherein each of the plurality of amplifier cells has a transconductance from the first input thereof to the output thereof, and

wherein each of the plurality of amplifier cells is selectively controllable in response to the control signal applied thereto to one of enable and disable each of the plurality of amplifier cells for adjusting a combined transconductance of the plurality of amplifier cells from the first inputs thereof to the outputs thereof.

48. (Previously Presented) The amplifier apparatus of claim 47, wherein each of the plurality of amplifier cells comprises at least one transistor.

49. (Previously Presented) The amplifier apparatus of claim 48, wherein each of the plurality of amplifier cells comprises a pair of transistors.

50. (Currently Amended) The amplifier apparatus of claim 49, wherein each pair of transistors comprises (i) a pair of input terminals, (ii) a pair of output terminals, and (iii) a pair of common terminals coupled to the control signal, and

wherein each of the amplifier cells includes first and second current sources respectively coupled to the pair of output terminals.

51. (Previously Presented) The amplifier apparatus of claim 49, wherein each of the pairs of transistors includes gates coupled in parallel, and wherein each of the pairs of transistors includes sources and drains coupled together to receive the control signal.

52. (Previously Presented) The amplifier apparatus of claim 47, wherein the transconductance of each of the plurality of amplifier cells is substantially identical.

53. (Previously Presented) The amplifier apparatus of claim 47, wherein the transconductance of at least one of the plurality of amplifier cells is different than the transconductance of other ones of the plurality of amplifier cells.

54. (Previously Presented) The amplifier apparatus of claim 47, wherein each of the plurality of amplifier cells comprises a controllable current source to adjust the transconductance of the amplifier cell in response to the control signal applied thereto.

55. (Currently Amended) The amplifier apparatus of claim 54, ~~wherein each of the plurality of amplifier cells further includes a common terminal, and~~ wherein the controllable current source of the amplifier cell is in communication with the ~~common terminal~~ second input.

56. (Previously Presented) An amplifier device, comprising:

a plurality of amplifier cells, each of the plurality of amplifier cells comprising at least one transistor,

wherein the plurality of amplifier cells are arranged in parallel,

wherein each of the plurality of amplifier cells includes an input terminal,

wherein the input terminal of each of the plurality of amplifier cells is in communication with input terminals of other ones of the plurality of amplifier cells,

wherein each of the plurality of amplifier cells includes an output terminal,

wherein the output terminal of each of the plurality of amplifier cells is in communication with output terminals of other ones of the plurality of amplifier cells, and

wherein each of the plurality of amplifier cells has a transconductance from an input thereof to an output thereof; and

means for selectively controlling each of the plurality amplifier cells to enable at least one of the plurality of amplifier cells for adjusting a combined transconductance of the amplifier device.

57. (Previously Presented) The amplifier device of claim 56, wherein each of the plurality of amplifier cells comprises a pair of transistors.

58. (Currently Amended) The amplifier device of claim 57, wherein each pair of transistors comprises (i) a pair of input terminals, (ii) a pair of output terminals, and (iii) a pair of common terminals connected together, and

wherein each of the amplifier cells includes first and second current sources respectively coupled to the pair of output terminals.

59. (Previously Presented) The amplifier device of claim 57, wherein each of the pairs of transistors includes gates coupled in parallel, and wherein each of the pairs of transistors includes sources and drains coupled together to receive a control signal.

60. (Previously Presented) The amplifier device of claim 56, wherein the transconductance of each of the plurality of amplifier cells is substantially identical.

61. (Previously Presented) The amplifier device of claim 56, wherein the transconductance of at least one of the plurality of amplifier cells is different than the transconductance of other ones of the plurality of amplifier cells.

62. (Currently Amended) An amplifier device, comprising:

a plurality of amplifier cells, wherein each of the plurality of amplifier cells comprises:

a pair of gain elements, wherein each of the pair of gain elements comprises:

i.) a pair of input terminals,

ii.) a pair of output terminals, and

iii.) a pair of common terminals connected together in communication with a control signal,

wherein the plurality of amplifier cells are arranged in parallel,

wherein each of the pair of input terminals of the plurality of amplifier cells are in communication with ~~a common source of~~ a control ~~signal~~ voltage and with the pairs of input terminals of other ones of the plurality of amplifier cells,

wherein each of the pair of output terminals of the plurality of amplifier cells are in communication with the pairs of output terminals of other ones of the plurality of amplifier cells,

wherein each of the plurality of amplifier cells has a transconductance from the input thereof to the output thereof, and

wherein each of the plurality of amplifier cells is selectively controllable in response to the control signal applied thereto to one of enable and disable each of the plurality of amplifier cells for adjusting a combined transconductance of the plurality of amplifier cells.

63. (Previously Presented) The amplifier device of claim 62, wherein each of the pair of gain elements comprises a pair of transistors.

64. (Previously Presented) The amplifier device of claim 63, wherein each of the pairs of transistors includes gates coupled in parallel, and wherein each of the pairs of transistors includes sources and drains coupled together to receive the control signal.

65. (Previously Presented) The amplifier device of claim 62, wherein each of the amplifier cells includes first and second current sources respectively coupled to the pair of output terminals.

66. (Previously Presented) The amplifier device of claim 62, wherein the transconductance of each of the plurality of amplifier cells is substantially identical.

67. (Previously Presented) The amplifier device of claim 62, wherein the transconductance of at least one of the plurality of amplifier cells is different than the transconductance of other ones of the plurality of amplifier cells.

68. (Previously Presented) The amplifier device of claim 62, wherein each of the plurality of amplifier cells comprises a controllable current source to adjust the transconductance of the amplifier cell in response to the control signal applied thereto.

69. (Previously Presented) The amplifier apparatus of claim 68, wherein the controllable current source in each of the plurality of amplifier cells is in communication with the corresponding pair of common terminals in each of the plurality of amplifier cells.

70. (Currently Amended) A method of controlling an amplifier apparatus, comprising the steps of:

providing a plurality of amplifier cells,

wherein each of the plurality of amplifier cells includes (i) ~~an~~ at least one first input in communication with a common ~~source of a~~ control ~~signal~~ voltage, (ii) a second input in communication with a control signal, and ~~(ii)~~ (iii) an output,

wherein the plurality of amplifier cells are arranged in parallel,

wherein the first input of each of the plurality of amplifier cells is in communication with the first inputs of other ones of the plurality of amplifier cells,

wherein the output of each of the plurality of amplifier cells is in communication with the outputs of other ones of the plurality of amplifier cells, and

wherein each of the plurality of amplifier cells has a transconductance from the first input thereof to the output thereof;

receiving the control signal ~~from the common source~~ at the second inputs of each of the plurality of amplifier cells; and

selectively controlling each of the plurality of amplifier cells in response to the received control signal to one of enable and disable each of the plurality of amplifier

cells to adjust a combined transconductance of the plurality of amplifier cells from the first inputs thereof to the outputs thereof.

71. (Previously Presented) The method of claim 70, wherein each of the plurality of amplifier cells includes at least one transistor.

72. (Previously Presented) The method of claim 70, wherein the transconductance of each of the plurality of amplifier cells is substantially identical.

73. (Previously Presented) The method of claim 70, wherein the transconductance of at least one of the plurality of amplifier cells is different than the transconductance of other ones of the plurality of amplifier cells.

74. (Previously Presented) A method of controlling an amplifier device, comprising the steps of:

providing a plurality of amplifier cells, each of the plurality of amplifier cells including at least one transistor,

wherein each of the plurality of amplifier cells includes an input terminal, wherein each of the plurality of amplifier cells includes an output terminal, and

wherein each of the plurality of amplifier cells has a transconductance from an input thereof to an output thereof;

arranging the plurality of amplifier cells in parallel,

wherein the input terminal of each of the plurality of amplifier cells is in communication with the input terminals of other ones of the plurality of amplifier cells, and

wherein the output terminal of each of the plurality of amplifier cells is in communication with the output terminals of other ones of the plurality of amplifier cells; and

selectively controlling each of the plurality amplifier cells to enable at least one of the plurality of amplifier cells to adjust a combined transconductance of the amplifier device.

75. (Previously Presented) The method of claim 74, wherein the transconductance of each of the plurality of amplifier cells is substantially identical.

76. (Previously Presented) The method of claim 74, wherein the transconductance of at least one of the plurality of amplifier cells is different than the transconductance of other ones of the plurality of amplifier cells.

77. (Currently Amended) A method for controlling an amplifier device, comprising the steps of:

providing a plurality of amplifier cells, wherein each of the plurality of amplifier cells comprises:

a pair of gain elements, wherein each of the pair of gain elements comprises:

i.) a pair of input terminals,

ii.) a pair of output terminals, and

iii.) a pair of common terminals connected together in communication with a control signal,

wherein each of the plurality of amplifier cells has a transconductance from the input thereof to the output thereof;

arranging the plurality of amplifier cells in parallel;

arranging each pair of input terminals of the plurality of amplifier cells in common with ~~a source of a control signal and with~~ the pairs of input terminals of other ones of the plurality of amplifier cells;

arranging each pair of output terminals of the plurality of amplifier cells in common with the pairs of output terminals of other ones of the plurality of amplifier cells; and

selectively controlling each of the plurality of amplifier cells in response to the control signal applied thereto to one of enable and disable each of the plurality of amplifier cells to adjust a combined transconductance of the plurality of amplifier cells.

78. (Previously Presented) The method of claim 77, wherein the transconductance of each of the plurality of amplifier cells is substantially identical.

79. (Previously Presented) The method of claim 77, wherein the transconductance of at least one of the plurality of amplifier cells is different than the transconductance of other ones of the plurality of amplifier cells.

80. (Currently Amended) An amplifier apparatus, comprising:

means for providing a plurality of amplifier cells,

wherein each of the plurality of amplifier cells includes (i) ~~an~~ at least one first input in communication with a common ~~source of a~~ control ~~signal~~ voltage, (ii) a second input in communication with a control signal, and ~~(ii)~~ (iii) an output,

wherein the plurality of amplifier cells are arranged in parallel,

wherein the first input of each of the plurality of amplifier cells is in communication with the first inputs of other ones of the plurality of amplifier cells,

wherein the output of each of the plurality of amplifier cells is in communication with the outputs of other ones of the plurality of amplifier cells, and

wherein each of the plurality of amplifier cells has a transconductance from the first input thereof to the output thereof;

means for receiving the control signal ~~from the common source~~ at each of the plurality of amplifier cells; and

means for selectively controlling each of the plurality of amplifier cells in response to the received control signal to one of enable and disable each of the plurality of amplifier cells to adjust a combined transconductance of the plurality of amplifier cells from the first inputs thereof to the outputs thereof.

81. (Previously Presented) The amplifier apparatus of claim 80, wherein each of the plurality of amplifier cells comprises at least one transistor.

82. (Previously Presented) The amplifier apparatus of claim 80, wherein the transconductance of each of the plurality of amplifier cells is substantially identical.

83. (Previously Presented) The amplifier apparatus of claim 80, wherein the transconductance of at least one of the plurality of amplifier cells is different than the transconductance of other ones of the plurality of amplifier cells.

84. (Previously Presented) An amplifier device, comprising:

means for providing a plurality of amplifier cells, each of the plurality of amplifier cells including at least one transistor,

wherein each of the plurality of amplifier cells includes an input terminal, wherein each of the plurality of amplifier cells includes an output terminal, and

wherein each of the plurality of amplifier cells has a transconductance from an input thereof to an output thereof;

means for arranging the plurality of amplifier cells in parallel,

wherein the input terminal of each of the plurality of amplifier cells is in communication with the input terminals of other ones of the plurality of amplifier cells, and

wherein the output terminal of each of the plurality of amplifier cells is in communication with the output terminals of other ones of the plurality of amplifier cells; and

means for selectively controlling each of the plurality amplifier cells to enable at least one of the plurality of amplifier cells to adjust a combined transconductance of the amplifier device.

85. (Previously Presented) The method of claim 84, wherein the transconductance of each of the plurality of amplifier cells is substantially identical.

86. (Previously Presented) The method of claim 84, wherein the transconductance of at least one of the plurality of amplifier cells is different than the transconductance of other ones of the plurality of amplifier cells.

87. (Currently Amended) An amplifier device, comprising:

means for providing a plurality of amplifier cells, wherein each of the plurality of amplifier cells comprises:

a pair of gain elements, wherein each of the pair of gain elements comprises:

i.) a pair of input terminals,

ii.) a pair of output terminals, and

iii.) a pair of common terminals <u>connected together in communication with a control signal</u>,

wherein each of the plurality of amplifier cells has a transconductance from the input thereof to the output thereof;

means for arranging the plurality of amplifier cells in parallel;

means for arranging each pair of input terminals of the plurality of amplifier cells in common with ~~a source of a control signal and with~~ the pairs of input terminals of other ones of the plurality of amplifier cells;

means for arranging each pair of output terminals of the plurality of amplifier cells in common with the pairs of output terminals of other ones of the plurality of amplifier cells; and

means for selectively controlling each of the plurality of amplifier cells in response to the control signal applied thereto to one of enable and disable each of the plurality of amplifier cells to adjust a combined transconductance of the plurality of amplifier cells.

88. (Previously Presented) The method of claim 87, wherein the transconductance of each of the plurality of amplifier cells is substantially identical.

89. (Previously Presented) The method of claim 87, wherein the transconductance of at least one of the plurality of amplifier cells is different than the transconductance of other ones of the plurality of amplifier cells.

90. (Currently Amended) An amplifier apparatus, comprising:

a plurality of amplifier cell means,

wherein each of the plurality of amplifier cell means includes (i) ~~an~~ at least one first input in communication with a common ~~source of a~~ control ~~signal~~ voltage, (ii) a second input in communication with a control signal, and ~~(ii)~~ (iii) an output,

wherein the plurality of amplifier cell means are arranged in parallel,

wherein the output of each of the plurality of amplifier cell means is in communication with the outputs of other ones of the plurality of amplifier cell means,

wherein the first input of each of the plurality of amplifier cell means is in communication with the first inputs of other ones of the plurality of amplifier cell means,

wherein each of the plurality of amplifier cell means has a transconductance from the first input thereof to the output thereof, and

wherein each of the plurality of amplifier cell means is selectively controllable in response to the control signal applied thereto to one of enable and disable each of the plurality of amplifier cell means for adjusting a combined transconductance of the plurality of amplifier cell means from the first inputs thereof to the outputs thereof.

91. (Previously Presented) An amplifier device, comprising:

a plurality of amplifier cell means, each of the plurality of amplifier cell means comprising at least one transistor,

wherein the plurality of amplifier cell means are arranged in parallel,

wherein each of the plurality of amplifier cell means includes an input terminal,

wherein the input terminal of each of the plurality of amplifier cell means is in communication with input terminals of other ones of the plurality of amplifier cell means,

wherein each of the plurality of amplifier cell means includes an output terminal,

wherein the output terminal of each of the plurality of amplifier cell means is in communication with output terminals of other ones of the plurality of amplifier cell means, and

wherein each of the plurality of amplifier cell means has a transconductance from an input thereof to an output thereof; and

means for selectively controlling each of the plurality amplifier cell means to enable at least one of the plurality of amplifier cell means for adjusting a combined transconductance of the amplifier device.

92. (Currently Amended) An amplifier apparatus with a controllable Gm, comprising:

a plurality of Gm cells,

wherein each of the plurality of Gm cells includes (i) ~~an~~ at least one first input in communication with a common ~~source of a~~ control ~~signal~~ voltage, (ii) a second input in communication with a control signal, and ~~(ii)~~ (iii) an output,

wherein the plurality of Gm cells are arranged in parallel,

wherein the first input of each of the plurality of Gm cells is in communication with the first inputs of other ones of the plurality of Gm cells,

wherein the output of each of the plurality of Gm cells is in communication with the outputs of other ones of the plurality of Gm cells, and

wherein each of the plurality of Gm cells is selectively controllable in response to the control signal applied thereto to one of enable and disable each of the plurality of Gm cells for adjusting a combined Gm of the plurality of Gm cells.

93. (Previously Presented) The amplifier apparatus of claim 92, wherein each of the plurality of Gm cells comprises at least one transistor.

94. (Previously Presented) The amplifier apparatus of claim 93, wherein each of the plurality of Gm cells comprises a pair of transistors.

95. (Currently Amended) The amplifier apparatus of claim 94, wherein each pair of transistors comprises (i) a pair of input terminals, (ii) a pair of output terminals, and (iii) a pair of common terminals connected together in communication with the control signal, and

wherein each of the Gm cells includes first and second current sources respectively coupled to the pair of output terminals.

96. (Previously Presented) The amplifier apparatus of claim 94, wherein each of the pairs of transistors includes gates coupled in parallel, and wherein each of the pairs of transistors includes sources and drains coupled together to receive the control signal.

97. (Previously Presented) The amplifier apparatus of claim 92, wherein the Gm of each of the plurality of Gm cells is substantially identical.

98. (Previously Presented) The amplifier apparatus of claim 92, wherein the Gm of at least one of the plurality of Gm cells is different than the Gm of other ones of the plurality of Gm cells.

99. (Previously Presented) The amplifier apparatus of claim 92, wherein each of the plurality of Gm cells comprises a controllable current source to adjust the Gm of the Gm cell in response to the control signal applied thereto.

100. (Currently Amended) The amplifier apparatus of claim 99, ~~wherein each of the plurality of Gm cells further includes a common terminal, and~~ wherein the controllable current source of the Gm cell is in communication with the ~~common terminal~~ second input.

101. (Previously Presented) An amplifier device with a controllable Gm, comprising:

a plurality of Gm cells, each of the plurality of Gm cells comprising at least one transistor,

wherein the plurality of Gm cells are arranged in parallel,

wherein each of the plurality of Gm cells includes an input terminal,

wherein the input terminal of each of the plurality of Gm cells is in communication with input terminals of other ones of the plurality of Gm cells,

wherein each of the plurality of Gm cells includes an output terminal,

wherein the output terminal of each of the plurality of Gm cells is in communication with output terminals of other ones of the plurality of Gm cells, and

means for selectively controlling each of the plurality Gm cells to enable at least one of the plurality of Gm cells for adjusting a combined Gm of the amplifier device.

102. (Previously Presented) The amplifier device of claim 101, wherein each of the plurality of Gm cells comprises a pair of transistors.

103. (Currently Amended) The amplifier device of claim 102, wherein each pair of transistors comprises (i) a pair of input terminals, (ii) a pair of output terminals, and (iii) a pair of common terminals connected together in communication with a control signal, and

wherein each of the Gm cells includes first and second current sources respectively coupled to the pair of output terminals.

104. (Previously Presented) The amplifier device of claim 102, wherein each of the pairs of transistors includes gates coupled in parallel, and wherein each of the pairs of transistors includes sources and drains coupled together to receive a control signal.

105. (Previously Presented) The amplifier device of claim 101, wherein the Gm of each of the plurality of Gm cells is substantially identical.

106. (Previously Presented) The amplifier device of claim 101, wherein the Gm of at least one of the plurality of Gm cells is different than the Gm of other ones of the plurality of Gm cells.

107. (Currently Amended) A method of controlling Gm, comprising the steps of:

providing a plurality of Gm cells,

wherein each of the plurality of Gm cells includes (i) ~~an~~ at least one first input in communication with a common ~~source of a~~ control ~~signal~~ voltage, (ii) a second input in communication with a control signal, and ~~(ii)~~ (iii) an output,

wherein the plurality of Gm cells are arranged in parallel,

wherein the first input of each of the plurality of Gm cells is in communication with the first inputs of other ones of the plurality of Gm cells,

wherein the output of each of the plurality of Gm cells is in communication with the outputs of other ones of the plurality of Gm cells; and

selectively controlling each of the plurality of Gm cells in response to the control signal applied thereto to one of enable and disable each of the plurality of Gm cells for adjusting a combined Gm of the plurality of Gm cells.

108. (Previously Presented) The method of claim 107, wherein the Gm of each of the plurality of Gm cells is substantially identical.

109. (Previously Presented) The method of claim 107, wherein the Gm of at least one of the plurality of Gm cells is different than the Gm of other ones of the plurality of Gm cells.

110. (Previously Presented) A method of controlling Gm, comprising the steps of:

providing a plurality of Gm cells, each of the plurality of Gm cells comprising at least one transistor,

arranging the plurality of Gm cells in parallel,

wherein each of the plurality of Gm cells includes an input terminal,

wherein the input terminal of each of the plurality of Gm cells is in communication with input terminals of other ones of the plurality of Gm cells,

wherein each of the plurality of Gm cells includes an output terminal,

wherein the output terminal of each of the plurality of Gm cells is in communication with output terminals of other ones of the plurality of Gm cells, and

selectively controlling each of the plurality Gm cells to enable at least one of the plurality of Gm cells for adjusting a combined Gm of the plurality of Gm cells.

111. (Previously Presented) The method of claim 110, wherein the Gm of each of the plurality of Gm cells is substantially identical.

112. (Previously Presented) The method of claim 110, wherein the Gm of at least one of the plurality of Gm cells is different than the Gm of other ones of the plurality of Gm cells.

113. (Currently Amended) An amplifier apparatus, comprising:

a plurality of amplifier cells,

wherein each of the plurality of amplifier cells includes (i) ~~an~~ at least one first input in communication with a common ~~source of a~~ control ~~signal~~ voltage, (ii) a second input in communication with a control signal, and ~~(ii)~~ (iii) an output,

wherein each of the plurality of amplifier cells has a transconductance from the input thereof to the output thereof, and

wherein each of the plurality of amplifier cells is selectively controllable in response to the control signal applied thereto to one of enable and disable each of the plurality of amplifier cells for adjusting a combined transconductance of the plurality of amplifier cells from the inputs thereof to the outputs thereof.

114. (Previously Presented) An amplifier device, comprising:

a plurality of amplifier cells, each of the plurality of amplifier cells comprising at least one transistor,

wherein the plurality of amplifier cells are arranged in parallel, and

wherein each of the plurality of amplifier cells has a transconductance from an input thereof to an output thereof; and

means for selectively controlling each of the plurality amplifier cells to enable at least one of the plurality of amplifier cells for adjusting a combined transconductance of the amplifier device.